Claims

[c1]   1. A photosensor element, comprising:

a photosensor, located to receive incoming light, and to create photo carriers based on said incoming light, said photosensor having a first capacitance per-unit area; and

a storage capacitance, selectively coupled to said photosensor, and having a second capacitance per-unit area which is at least two orders of magnitude larger than the first capacitance per unit area of the photodiode.
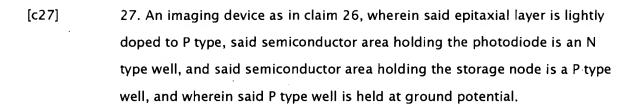
[c2]   2. An element as in claim 1, further comprising a controllable gate, coupled between said photosensor and said storage capacitance, which is selectively actuated to transfer a signal from said photosensor to said storage capacitance.

[c3]   3. An element as in claim 1, further comprising a light shield element, located to shield said storage capacitance against incoming light.

[c4]   4. An element as in claim 1, further comprising a reset structure, which operates to reset values in said photosensor and said storage capacitance, based on applied control signals.

[c5]   5. An element as in claim one, wherein said photosensor has a capacitance C_P, said storage capacitance has a capacitance C_D, and a value α is defined as C_P / C_D, and wherein said value α is > 0.7.

[c6]   6. An element as in claim 5, wherein said value α is > 0.9.

[c7]   7. An element as in claim 1, wherein said second capacitance per-unit area is at least ten times greater than said first capacitance per-unit area.

[c8]   8. An element as in claim 1, wherein said photosensor includes a photodiode.

[c9]   9. An element as in claimed 8, further comprising a semiconductor region forming an n well, holding said photodiode, and a second semiconductor region forming a P well, holding said storage capacitance.

[c10]   10. An element as in claim 9, further comprising a P type lightly doped epitaxial layer, underlying both said first semiconductor region and said second semiconductor region.

[c11]   11. An element as in claim 9, wherein said photodiode is formed as an N++ region within said n well, and said storage capacitance is formed as an N++ region within said P well.

[c12]   12. An element as in claim 11, further comprising a transfer gate, formed on the semiconductor substrate, and extending between the first N++ region and the second N++ region.

[c13]   13. An element as in claim 9, further comprising a metal shield, formed over at least a portion of said P well and shielding said storage node against incoming light.

[c14]   14. An element as in claim 9, further comprising a bias applied to said P. well that prevents photo carriers from reaching said storage node.

[c15]   15. An element as in claim 14, wherein said bias includes grounding said P well, and holding said N well at a bias above ground.

[c16]   16. An imaging device, comprising:

a semiconductor substrate;

a photodiode, formed in said semiconductor substrate, and having a capacitance C_D;

a selective connection between said photodiode and a reset node;

a storage capacitance, formed in said semiconductor substrate, and having a capacitance C_P;

a second switch, selectively connecting said storage capacitance to a reset node; and

a third switch, connected between said photodiode and said storage capacitance, and selectively actuated to provide photocarriers from said photodiode to said storage capacitance,

wherein said photodiode and said storage capacitance are formed such that

a ratio $\alpha = C_P / C_D$ is > 0.7.

[c17]   17. An imaging device as in claim 16,wherein said third switch includes a transfer gate.

[c18]   18. An imaging device as in claim 16, further comprising a light shield, covering said storage capacitance.

[c19]   19. An imaging device as in claim 16, wherein said ratio α is > 0.9.

[c20]   20. An imaging device as in claim 16, further comprising a bias element providing an electrical shield to cover said storage capacitance against photoelectrons.

[c21]   21. An imaging device as in claim 20, wherein said bias element includes biasing a semiconductor area holding the photodiode at a higher level then a bias of the semiconductor area holding the storage node.

[c22]   22. An imaging device as in claim 20, wherein said biasing element biases the semiconductor area holding the storage node to ground, and biases the semiconductor area holding the photodiode to a level above ground.

[c23]   23. An imaging device as in claim 20, wherein said bias element includes reverse biasing a semiconductor element forming said photodiode to prevent holes from reaching said photodiode.

[c24]   24. An imaging device as in claim 23, further comprising a contact located to drain holes away from said storage capacitance.

[c25]   25. An imaging device as in claim 21, wherein the semiconductor area holding the photodiode is a separate well from the semiconductor area holding the storage node, the two wells having opposite doping types.

[c26]   26. An imaging device as in claim 25, further comprising an epitaxial layer, on which the semiconductor areas holding the photodiode and the semiconductor area holding the storage node are both formed.
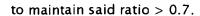
[c27]   27. An imaging device as in claim 26, wherein said epitaxial layer is lightly doped to P type, said semiconductor area holding the photodiode is an N type well, and said semiconductor area holding the storage node is a P type well, and wherein said P type well is held at ground potential.

[c28]   28. An imaging device as in claim 27, wherein a capacitance per-unit area of said storage node is at least two orders of magnitude higher than a capacitance per-unit area of said photodiode.

[c29]   29. An imaging device as in claim 16, wherein a capacitance per-unit area of said storage node is at least two orders of magnitude higher than a capacitance per-unit area of said photodiode.

[c30]   30. An imaging device as in claim 29, further comprising a plurality of additional photo sensors, forming an array of photo sensors.

[c31]   31. A photosensor, comprising:
a first substrate doped to with a P++ doping type;
a P. type epitaxial layer, lightly doped with P type impurities, formed on top of said P++ substrate;
an active semiconductor area, located on said P type epitaxial layer, and including an N type well holding a photodiode therein as an N++ type section within said N well, and a P type well, holding a storage node therein, as an N++ type portion within the P type well, and a transfer gate, extending between said N++ type photodiode, and said N++ type storage node, wherein a capacitance per-unit area of said storage node is much greater than a capacitance per-unit area of said photodiode.

[c32]   32. A photosensor as in claim 31, wherein said capacitance per-unit area of said storage node is at least two orders of magnitude greater than the capacitance per-unit area of said photodiode.

[c33]   33. A photosensor as in claim 32, further comprising defining a ratio between a capacitance of said storage node and a capacitance of said photodiode, and wherein said storage node and said photodiode are formed

to maintain said ratio > 0.7.

[c34]   34. A photosensor as in claim 31, further comprising a shielding element,
          located on top of said storage node, to shield said storage node against
          reception of incoming light.

[c35]   35. A photosensor as in claim 31, further comprising a bias connection that
          provides a field around said storage node that prevents photo carriers in
          adjacent areas from entering said storage node.

[c36]   36. A photosensor as in claim 35, wherein said field is formed by holding
          said P well at a lower bias than a bias of said N well, and said P. type
          epitaxial layer.

[c37]   37. A photosensor as in claim 35, wherein said photocarriers include at least
          photoelectrons and holes.

[c38]   38. A method, comprising:
          forming an array of photodetector elements, including a plurality of pixels,
          forming each pixel including a photodiode in a first semiconductor area, and
          forming a storage node for said photodiode in a second semiconductor area,
          separate from said first semiconductor area;
          operating said photodiode and storage node in a snapshot mode, where all
          pixels are sampled from said photodiode to said storage node at the same
          time; and
          biasing said storage node in a way that prevents photo carriers from outside
          said storage node from entering said storage node.

[c39]   39. A method as in claim 38, wherein said biasing prevents photo electrons
          from entering said second semiconductor area.

[c40]   40. A method as in claim 38, wherein said biasing prevents holes from
          entering said storage node.

[c41]   41. A method as in claim 40, further comprising an electrode that draws
          holes away from said storage node.

[c42]   42. A method comprising:

reading all pixel values in an imaging device simultaneously into respective

in-pixel storage devices; and

In each said pixel, erecting both optical and diffusion shields for the in pixel

storage devices.